CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a single semiconductor substrate having thereon a surface region;

at least one non-MODFET transistor; and

a MODFET, wherein said MODFET, and said at least one non-MODFET transistor, are formed on said single semiconductor substrate, and wherein an intrinsic region for said MODFET is formed in a groove in the surface region, and wherein the groove is formed by a side wall and a bottom.

2. The semiconductor device of claim 1, wherein a first height of a first portion of the surface region whereon said non-MODFET transistor is resident is approximately equal to a second height of a second portion of the surface region whereon the intrinsic region is resident.

3. The semiconductor device of claim 2, further comprising:

an insulation film formed on the side wall of the groove.

4. The semiconductor device of claim 3, wherein the groove has a rectangular planer shape, and wherein a direction of one face of the rectangle plane is [110] co-planar with a crystal orientation of said single semiconductor substrate.

5. The semiconductor device of claim 3, wherein said insulation film comprises a silicon nitride film.

6. The semiconductor device of claim 1, wherein the intrinsic region comprises:

a multi-layered film, comprising:

a buffer layer;

a single-crystal silicon layer laminated on the buffer layer; and

a single-crystal silicon-germanium layer laminated on the buffer layer.

7. The semiconductor device of claim 6, wherein said MODFET comprises a P-type MODFET, and wherein the multi-layered film comprises:

a carrier supply layer comprising a single-crystal silicon-germanium containing a P-type dopant;

a spacer layer comprising a single-crystal silicon-germanium;

a channel layer comprising an undoped single-crystal silicon-germanium; and

a cap layer comprising a single-crystal silicon.

8. The semiconductor device of claim 6, wherein said MODFET comprises a P-type MODFET, and wherein the multi-layered film comprises:

a first spacer layer comprising a single silicon-germanium;

a channel layer comprising an undoped single-crystal silicon-germanium;

a second spacer layer comprising a single-crystal silicon-germanium;

a carrier supply layer comprising a single-crystal silicon-germanium including a P-type dopant; and

a cap layer comprising a single-crystal silicon.

9. The semiconductor device of claim 7 or 8, wherein the channel layer comprises a single-crystal silicon-germanium undergoing compressive strain.

10. The semiconductor device of claim 6, wherein said MODFET comprises an N-type MODFET, and wherein the multi-layered film comprises:

a first spacer layer comprising a single silicon-germanium;

a channel layer comprising an undoped single crystal;

a second spacer layer comprising a single-crystal silicon-germanium;

a carrier supply layer comprising a single-crystal silicon-germanium including an N-type

dopant; and

a cap layer comprising a single-crystal silicon.

11. The semiconductor device of claim 6, wherein said MODFET is an N-type MODFET, and wherein the multi-layered film comprises:

a carrier supply layer comprising a single-crystal silicon-germanium containing an N-type dopant;

a first spacer layer comprising a single-crystal silicon-germanium;

a channel layer comprising an undoped single-crystal silicon;

a second spacer layer comprising a single-crystal silicon-germanium; and

a cap layer comprising a single-crystal silicon.

12. The semiconductor device of claim 10 or 11, wherein the channel layer comprises a single-crystal silicon undergoing tensile strain.

13. A semiconductor device, comprising:

a single semiconductor substrate having a surface region;

an SiGeHBT, having a collector layer formed on said single semiconductor substrate; and

a MODFET, having a buffer layer formed on said single semiconductor substrate;

wherein the collector layer is formed in a first groove on the semiconductor substrate, and wherein the buffer layer is formed in a second groove on the semiconductor substrate.

14 The semiconductor device of claim 13, wherein a first height of a first portion of the surface region whereon the collector layer is resident is approximately equal to a second height of a second portion of the surface region whereon the buffer layer is resident.

15. The semiconductor device of claim 14, further comprising an insulation film formed on a side wall of the second groove.

16. The semiconductor device of claim 15, wherein the second groove has a rectangular planer shape, and wherein an direction of one face of the rectangle plane is [110] co-planar with a crystal orientation of said single semiconductor substrate.

17. The semiconductor device of claim 15, wherein said insulation film comprises silicon nitride.

18. The semiconductor device of claim 13, further comprising:

a multi-layered film, comprising:

a single-crystal silicon and a single-crystal silicon-germanium laminated on the buffer layer and on the collector layer, wherein said MODFET comprises a P-type, and wherein said SiGeHBT comprises an NNP-type.

19. The semiconductor device of claim 18, wherein said multi-layered film comprises:

a first spacer layer comprising the single-crystal silicon-germanium;

a carrier supply layer comprising the single-crystal silicon-germanium and including a P-type dopant;

a second spacer layer comprising the single-crystal silicon or the single-crystal silicon-germanium;

a channel layer comprising the single-crystal silicon-germanium undoped; and

a cap layer comprising the single-crystal silicon.

20. The semiconductor device of claim 19, wherein the channel layer comprises the single-crystal silicon-germanium undergoing compressive strain.

21. A method of manufacturing a semiconductor device having a MOSFET and an MODFET on a single semiconductor substrate, comprising:

forming, on the semiconductor substrate, a single-crystal silicon including a device

isolation insulation film;

covering the semiconductor substrate in a MOSFET forming region with the device isolation insulation film;

forming a groove in which the device isolation insulation film is exposed, and the single-crystal silicon is exposed, in a MODFET forming region;

forming, in the groove, an intrinsic region for the MODFET in the groove using selective growth;

forming a gate insulation film and a gate electrode for the MOSFET; and

forming a gate insulation film and a gate electrode for the MODFET.

22. The method of claim 21, further comprising:

forming a silicon nitride film on a lateral surface of the groove.

23. The method of claim 21, further comprising:

selective growth of a buffer layer comprising a single-crystal silicon-germanium on a single-crystal silicon;

wherein the MODFET is a P-type, and wherein said forming, in the groove, an intrinsic region for the MODFET comprises:

selective growth of a carrier supply layer comprising a single-crystal silicon-germanium doped with a P-type dopant, a spacer layer comprising a single-crystal silicon-germanium, a channel layer comprising a single-crystal silicon-germanium, and a cap layer comprising a single-crystal silicon, successively on the buffer layer.

24. The method of claim 23, wherein the germanium content of the channel layer is higher than the germanium content of the spacer layer.

25. The method of claim 21, wherein the MODFET is a P-type, further comprising:

selective growth of a buffer layer comprising a single-crystal silicon-germanium on a single-crystal silicon;

wherein said forming, in the groove, an intrinsic region for the MODFET comprises:

selective growth of a first spacer layer comprising a single-crystal silicon-germanium, a channel layer comprising a single-crystal silicon-germanium, a second spacer layer comprising a single-crystal silicon-germanium, a carrier supply layer comprising a single-crystal silicon-germanium doped with a P-type dopant, and a cap layer comprising a single-crystal silicon, successively on the buffer layer.

26. The method of claim 25, wherein the germanium content of the channel layer is higher than the germanium content of the first spacer layer.

27. The method of claim 21, wherein the MODFET is an N-type, further comprising:

selective growth of a buffer layer comprising a single-crystal silicon-germanium on a single-crystal silicon;

wherein said forming, in the groove, an intrinsic region for the MODFET comprises:

selective growth of a first spacer layer comprising a single-crystal silicon-germanium, a channel layer comprising a single-crystal silicon, a second spacer layer comprising a single-crystal silicon-germanium, and a cap layer comprising a single-crystal silicon, successively on the buffer layer single-crystal silicon.

28. The method of claim 21, wherein the MODFET is an P-type, further comprising:

selective growth of a buffer layer comprising a single-crystal silicon-germanium on a single-crystal silicon;

wherein said forming, in the groove, an intrinsic region for the MODFET comprises:

selective growth of a carrier supply layer comprising a single-crystal silicon-germanium doped with an N-type dopant, a first spacer layer comprising a single-crystal silicon-germanium, a channel layer comprising a single-crystal silicon containing no dopant, a second spacer layer comprising a single-crystal silicon-germanium, and a cap layer comprising a single-crystal silicon, successively on the buffer layer single-crystal silicon.

29. The method of claim 21, wherein said forming, in the groove, an intrinsic region for the MODFET comprises conducting a CVD including a halogenous gas.

30. The method of claim 29, wherein a source gas for silicon comprises at least one selected from the group consisting of silicon hydride and chloride, and wherein a source gas for germanium comprises at least one selected from the group consisting of germanium hydride and chloride, and wherein the halogenous gas comprises a hydrogen chloride gas of flow rate in a range of about 20 to about 80 ml/min.

31. The method of claim 21, wherein said forming, in the groove, an intrinsic region for the MODFET comprises conducting a gas source MBE including a halogenous gas.

32. The method of claim 31, wherein disilane is a source gas for silicon, and wherein germane is a source gas for germanium, and wherein a hydrogen chloride gas is the halogenous gas, and wherein the flow rate of the hydrogen chloride gas is in a range of about 5 to about 10 ml/min.

33. A method of manufacturing a semiconductor device having an SiGeHBT and an MODFET on one semiconductor substrate, comprising:

growing a single-crystal silicon-germanium over a single-crystal silicon on the semiconductor substrate;

etching, after said growing a single-crystal silicon-germanium on the semiconductor substrate, to thereby form a collector layer of the SiGeHBT and a buffer layer of the MODFET;

depositing an insulation film;

partially removing the insulation film to expose an upper surface of the collector layer and on upper surface of the buffer layer;

selective growth of a multi-layered film, including a single-crystal silicon and a single-

crystal silicon-germanium, on the upper surface of the collector layer and on the upper surface of the buffer layer; and

forming an emitter electrode of the SiGeHBT, and a gate insulation film and a gate electrode of the MODFET, on the multi-layered film.

34. The method of claim 33, wherein said selective growth of a multi-layered film, including a single-crystal silicon and a single-crystal silicon-germanium, comprises:

forming a first, a second, a third and a fourth single-crystal silicon-germanium layer, and at least one single-crystal silicon layer, from the collector layer and from the buffer layer, wherein a dopant is added to the second single-crystal silicon-germanium layer.

35. The method of claim 34, wherein the first and second single-crystal silicon-germanium layers at the SiGeHBT form a base layer of the SiGeHBT, and wherein the third and fourth single-crystal silicon-germanium layers, and the single-crystal silicon layers, at the SiGeHBT form an emitter layer of the SiGeHBT.

36. The method of claim 34, wherein the first single-crystal silicon-germanium layer forms a first spacer layer, wherein the second single-crystal silicon-germanium layer forms a carrier supply layer, wherein the third single-crystal silicon-germanium layer forms a second spacer layer, wherein the fourth single-crystal silicon-germanium layer forms a channel layer, and wherein at least one of the at least one single-crystal silicon layer forms a cap layer at the MODFET.

37. The method of claim 33, wherein said selective growth of a multi-layered film, including a single-crystal silicon and a single-crystal silicon-germanium, comprises a CVD including a halogenous gas.

38. The method of claim 37, wherein a source gas for silicon comprises at least one selected from the group consisting of silicon hydride and chloride, and wherein a source gas

for germanium comprises at least one selected from the group consisting of germanium hydride and chloride, and wherein the halogenous gas comprises a hydrogen chloride gas of flow rate in a range of about 20 to about 80 ml/min.

39. The method of claim 33, wherein said selective growth of a multi-layered film, including a single-crystal silicon and a single-crystal silicon-germanium, comprises conducting a gas source MBE including a halogenous gas.

40. The method of claim 39, wherein disilane is a source gas for silicon, and wherein germane is a source gas for germanium, and wherein a hydrogen chloride gas is the halogenous gas, and wherein the flow rate of the hydrogen chloride gas is in a range of about 5 to about 10 ml/min.

41. A method of manufacturing a semiconductor device having an SiGeHBT and an MODFET on one semiconductor substrate comprising:

forming a semiconductor substrate having a single-crystal silicon including therein a device isolation insulation film and a collector layer of the SiGeHBT;

covering a MODFET forming region with an insulation film;

forming a groove wherein the device isolation insulation film is exposed from a side wall, and wherein the single-crystal silicon is exposed from a bottom surface;

selective growth of an intrinsic region for the MODFET in the groove; and

forming an emitter electrode of the SiGeHBT, and a gate insulation film and a gate electrode of the MODFET.

42. The method of claim 41, wherein the MODFET is a P-type, further comprising:

selective growth of a buffer layer comprising a single-crystal silicon-germanium on a single-crystal silicon;

wherein said selective growth of an intrinsic region for the MODFET in the groove comprises:

selective growth of a carrier supply layer comprising a single-crystal silicon-germanium doped with a P-type dopant, a spacer layer comprising a single-crystal silicon-germanium, a channel layer comprising a single-crystal silicon-germanium, and a cap layer comprising a single-crystal silicon, successively on the buffer layer single-crystal silicon.

43. The method of claim 42, wherein the germanium content of the channel layer is higher than the germanium content of the spacer layer

44. The method of claim 41, wherein the MODFET is an P-type, further comprising:

selective growth of a buffer layer comprising a single-crystal silicon-germanium on a single-crystal silicon;

wherein said selective growth of an intrinsic region for the MODFET in the groove comprises:

selective growth of a first spacer layer comprising a single-crystal silicon-germanium, a channel layer comprising a single-crystal silicon-germanium, a second spacer layer comprising a single-crystal silicon-germanium, a carrier supply layer comprising a single-crystal silicon-germanium doped with a P-type dopant, and a cap layer comprising a single-crystal silicon, successively on the buffer layer single-crystal silicon.

45. The method of claim 44, wherein the germanium content of the channel layer is higher than the germanium content of the first spacer layer.

46. The method of claim 41, wherein the MODFET is an N-type, further comprising:

selective growth of a buffer layer comprising a single-crystal silicon-germanium on a single-crystal silicon;

wherein said selective growth of an intrinsic region for the MODFET in the groove comprises:

selective growth of a first spacer layer comprising a single-crystal silicon-germanium, a channel layer comprising a single-crystal silicon, a second spacer layer comprising a single-crystal silicon-germanium, a carrier supply layer comprising a single-crystal silicon-germanium doped with an N-type dopant, and a cap layer comprising a single-crystal silicon, successively on the buffer layer.

47. The method of claim 41, wherein the MODFET is an N-type, further comprising:

selective growth of a buffer layer comprising a single-crystal silicon-germanium on a single-crystal silicon;

wherein said selective growth of an intrinsic region for the MODFET in the groove comprises:

selective growth of a carrier supply layer comprising a single-crystal silicon-germanium doped with an N-type dopant, a first spacer layer comprising a single-crystal silicon-germanium, a channel layer comprising a single-crystal silicon, a second spacer layer comprising a single-crystal silicon-germanium, and a cap layer comprising a single-crystal silicon, successively on the buffer layer.

48. The method of claim 41, wherein said selective growth of an intrinsic region for the MODFET in the groove comprises conducting a CVD including a halogenous gas.

49. The method of claim 48, wherein a source gas for silicon comprises at least one selected from the group consisting of silicon hydride and chloride, and wherein a source gas for germanium comprises at least one selected from the group consisting of germanium hydride and chloride, and wherein the halogenous gas comprises a hydrogen chloride gas of flow rate in a range of about 20 to about 80 ml/min.

50. The method of claim 41, wherein said selective growth of an intrinsic region for the MODFET in the groove comprises conducting a gas source MB including a halogenous gas.

51. The method of claim 50, wherein disilane is a source gas for silicon, and wherein germane is a source gas for germanium, and wherein a hydrogen chloride gas is the halogenous gas, and wherein the flow rate of the hydrogen chloride gas is in a range of about 5 to about 10 ml/min.